*DSP TMS320C3x SERIES*

PCI BUS

## 4-Channel High Speed Data Acquisition

# DMP1162B

## Hardware Manual



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# Chapter 1
# Introduction

The DMP1162B is a digital signal processor (DSP) board based on the Texas Instruments TMS320C31 processor, manufactured by DongMyung Electronics, Co. and designed by Korea Atomic Energy Research Institute.

The board is capable of fast digital signal processing such as averaging, RMS(Root Mean Square), FFT(Fast Fourier Transform), filter functions, etc.
Also, The board is also capable of acquiring the data from analog signals such as temperature, flow, pressure, acoustic wave, etc.
The board is compatible with the industrial PCI bus interface and is capable of both bus master and slave transactions on the host bus.
The DMP1162B is appropriate to data acquisition and control tasks.
The DMP1162B is also capable of I/O slave to support the existing TMS320C3X processor system.

The DMP1162B features include:

1) TMS320C31 processor (40MHz)
2) Single SRAM memory pool
3) PCI bus interface
4) Two channels of on-board timer
5) 200KHz Sample x 4 channel ADC input
6) 16Bits x 1KB FIFO Memory

If you have any questions about hardware circuit of the DMP1162B board, contact to DongMyung Electronics.

# Chapter 2
# Installation

This chapter describes how to install Hardware and Vxd of DMP1162B and verify hardware and VxD of DMP1162B. Chapter contains

# 2.1 Installing Hardware

## 2.1.1 System Requirements ( PC Specification )

Table 1-1 System Requirements

| Item | Spec. |
|---|---|
| CPU | As minimum, Pentium 300MHz is required. IBM PC Compatible |
| Memory | As minimum, 64M Byte is required |
| Monitor | Resolution 1024 x 768 |
| HDD | As minimum, 2 GIGA byte is required |
| misc. | 3.5 " FDD, CD-ROM |

## 2.1.2 Hardware Install

Follow the procedures below to install the DMP1162B board.

1. Turn "OFF" the computer power
2. Remove the computer case.
3. Clean PCI slot.
4. Insert DMP1162B board to PCI slot of the computer.
5. Turn "ON" the computer.

### 2.1.3 Hardware Connection

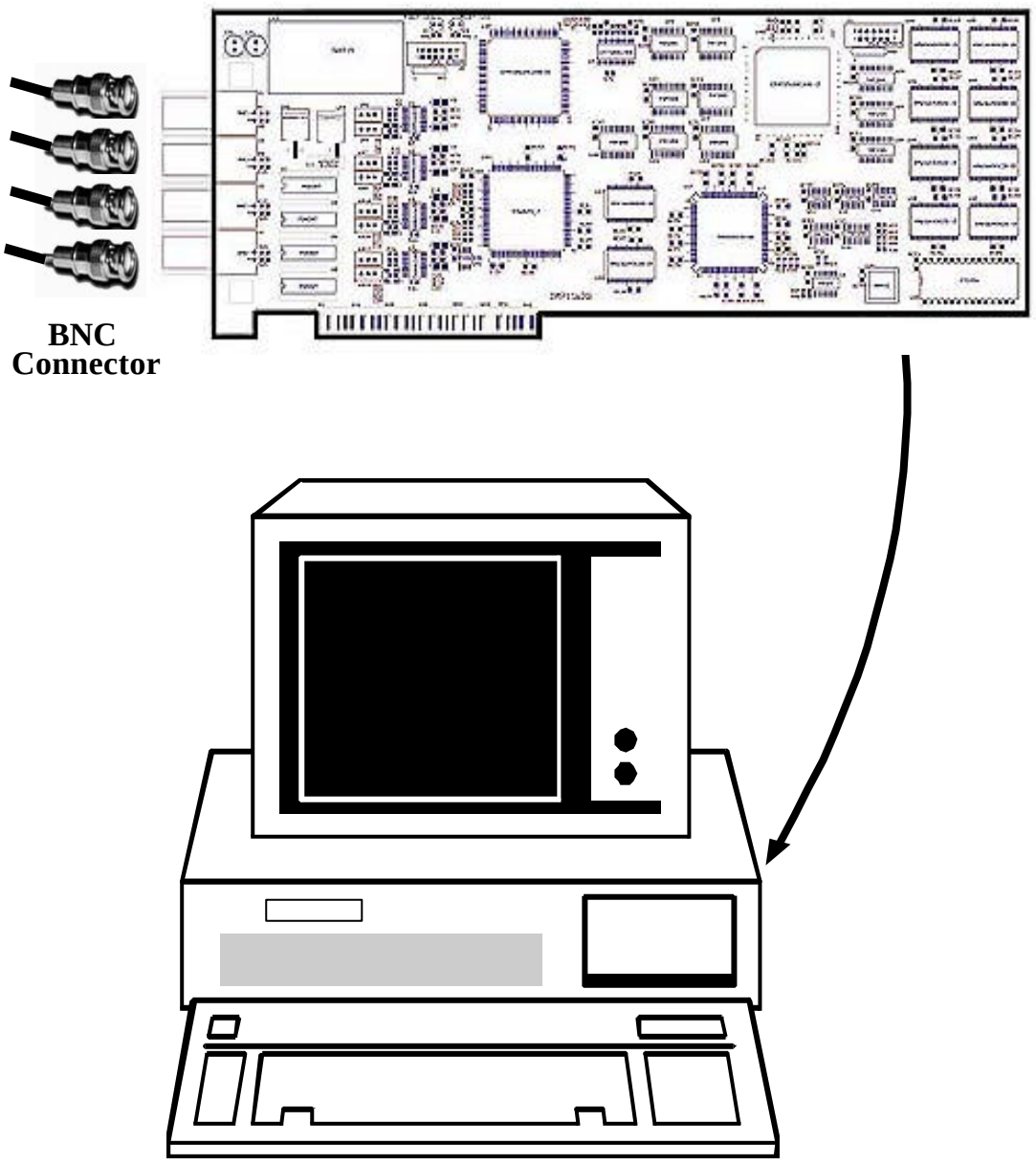
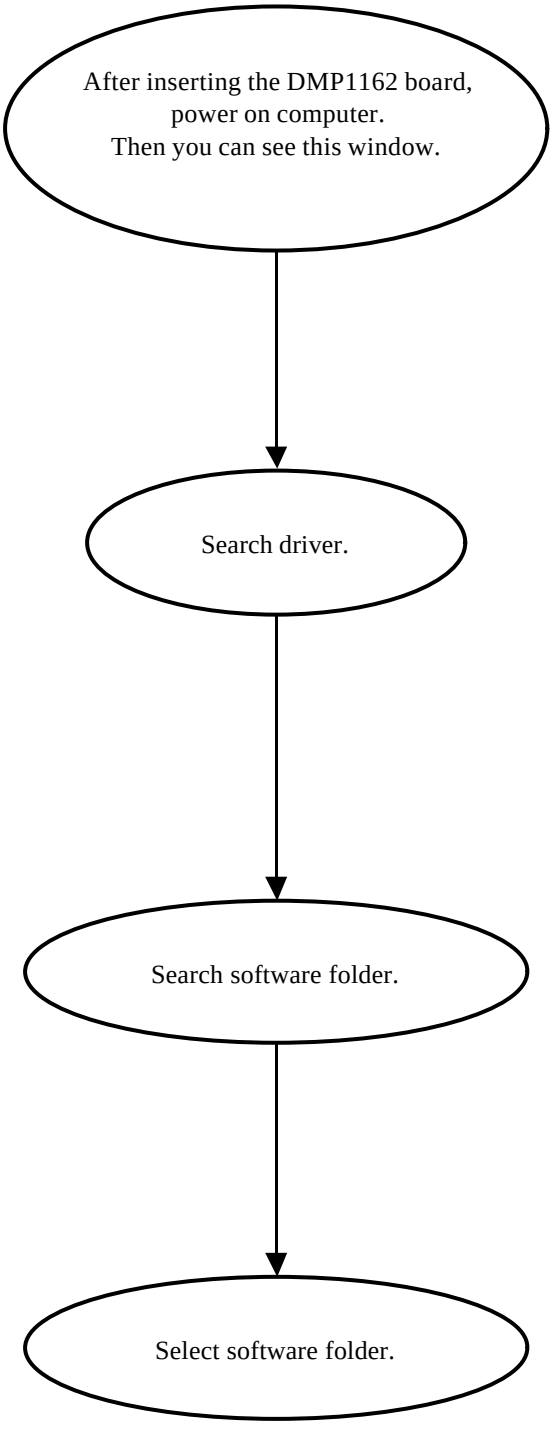


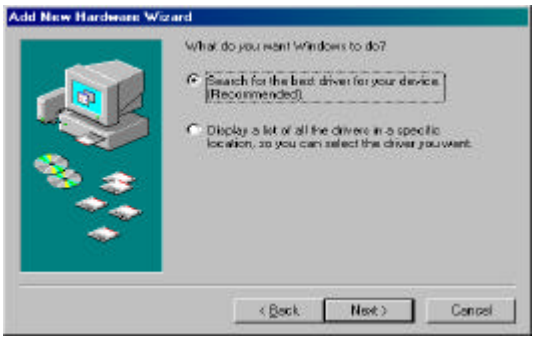

Figure 2-1 Hardware Wiring

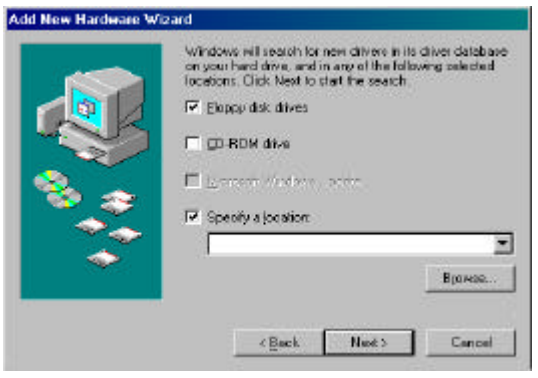
## 2.2 Installing and Verifying VxD

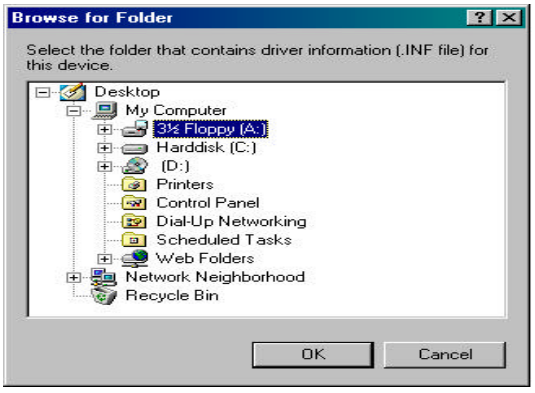
### 2.2.1 Installing VxD







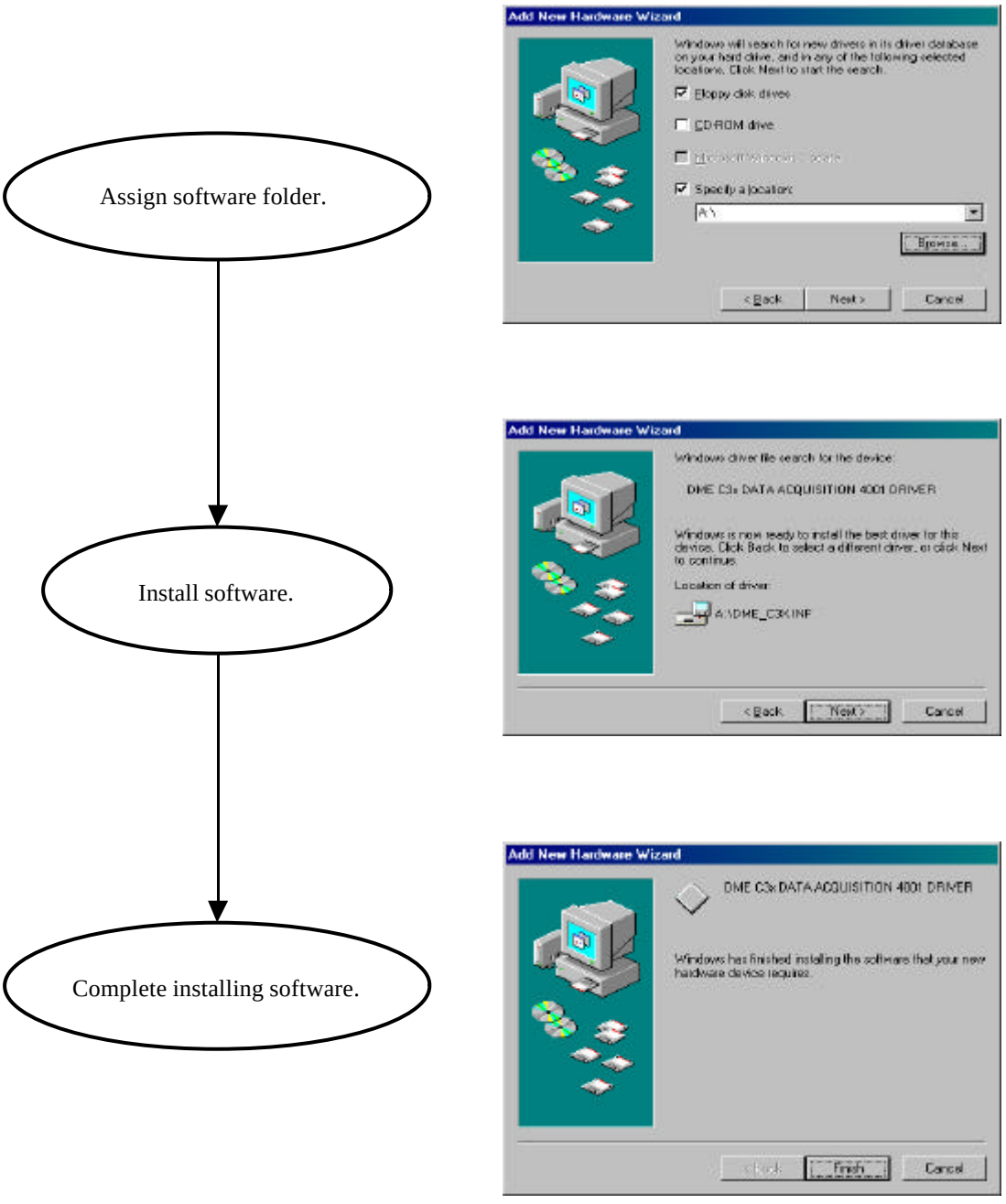
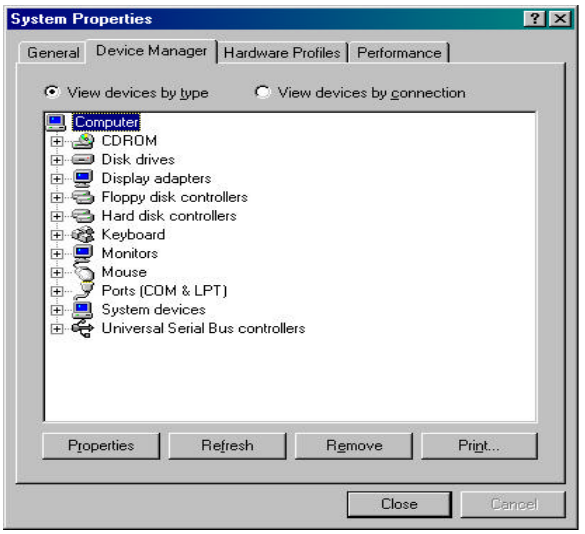



Figure 2-2 Installing VxD

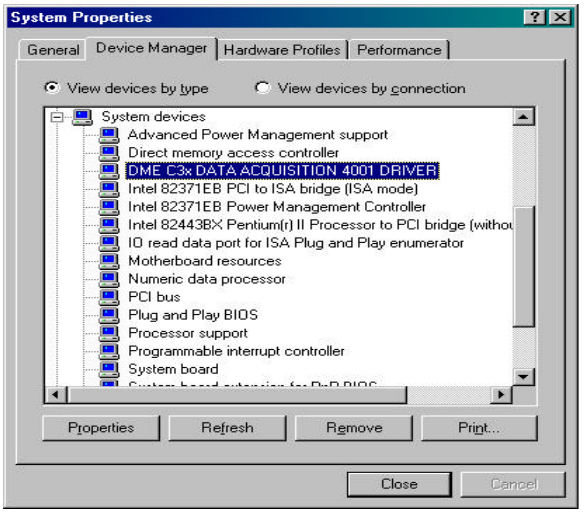
## 2.2.2 Verifying VxD and Hardware

Select menu to below.
Start Menu -> Setting ->
Control Panel -> System

Click "Device Manager".
Then you can see this window.




Select "DME C3x DATA ACQUISITION DRIVER", and click it.




Click resource among menu.
The kinds of resource and Setting value will be displayed.
( You can see different setting value in case that they have different PC. )
Hardware and VxD is installed properly if one interrupt and two memory space are set.

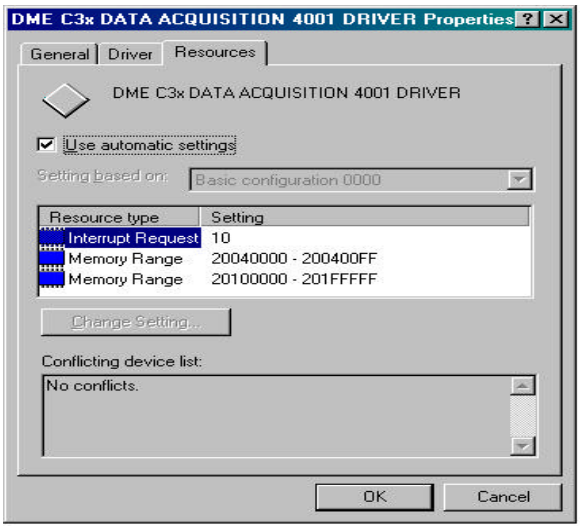



Figure 2-3 Verifying VxD and Hardware

# Chapter 3
# Hardware Description

This chapter describes board configuration, It's detail functions, VHDL, firmware and VxD of DMP1162B Chapter contains

## 3.1 Board Configuration

### 3.1.1 Board Layout

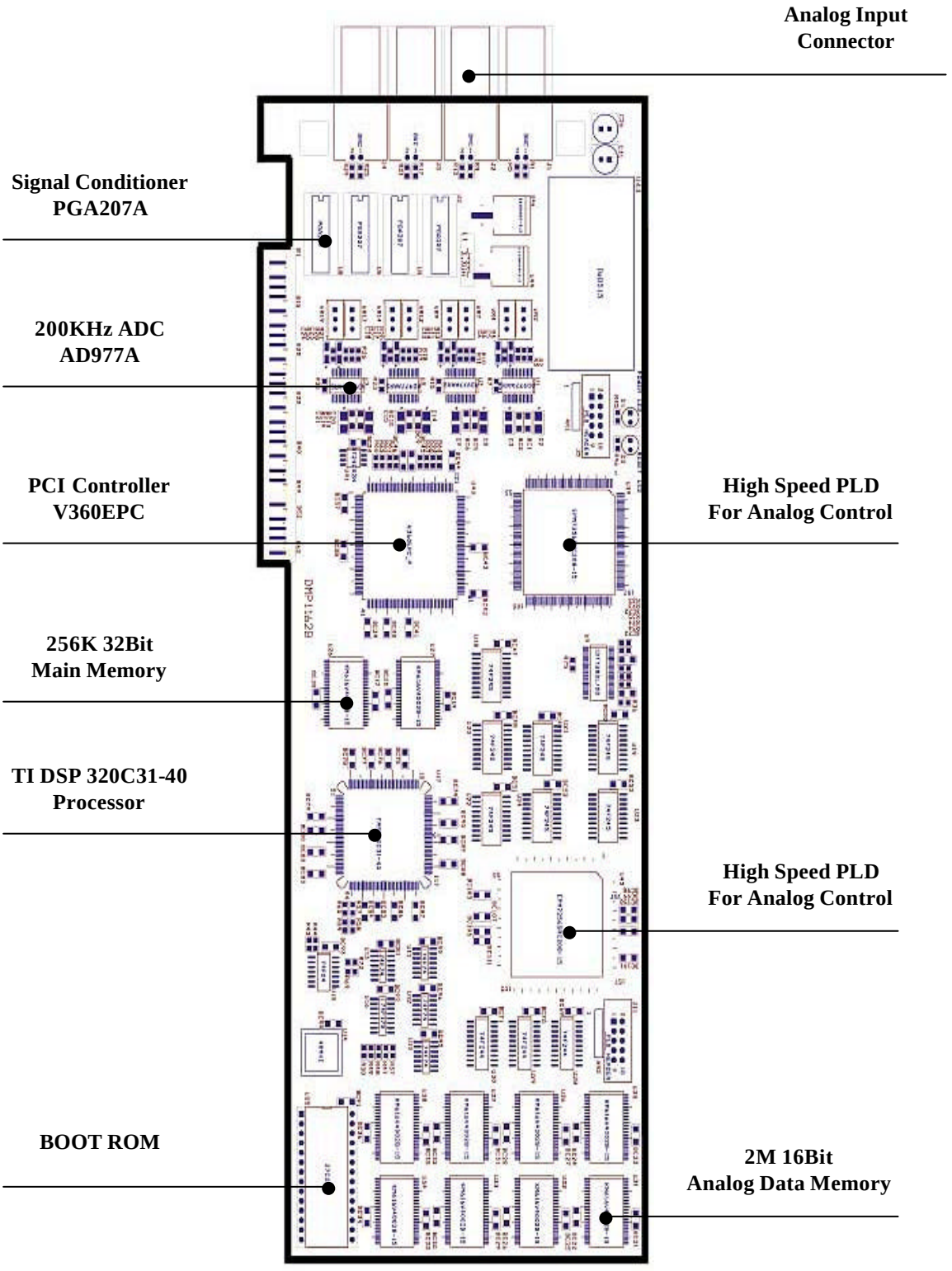



Figure 3-1 Board Layout

### 3.1.2 General Specification

Table 3-1 General Specification

| Item | Spec. | Note |
|---|---|---|
| 1. Processor | 1. CPU : DSP-TMS320C31<br>2. Speed : 40 MHz<br>3. Serial Port : 1 Port | |
| 2. Processor Memory | 1. Program Memory : 256KByte * 32 Bits<br>2. Analog Data Memory : 2MByte * 16 Bits | |
| 3. Fifo Memory | 1. Size : 1K * 16 Bits | |
| 4. Command Port | 1. 32Bits | |
| 5. Data Port | 1. 32Bits | |
| 6. A/D Converter | 1. Chip :AD977A<br>2. Resolution : 16 Bit (Include Sign Bit )<br>3. Input Range : -10V ~ +10V<br>4. Maximum Reading Rate : 200KSample/sec | |
| 7. Signal Conditioner | 1. Chip :PGA207P<br>2. Input Voltage Protection : -40V ~ +40V<br>3. Input Impedance : $10^{13}$Ohm 1pF<br>4. Gain = 1, 2, 5, 10V/V | |
| 8. Power Supply | +5, -5, +15, -15 Volt | |
| 9. PCB | 305x114mm 6 layer epoxy resins board | |

## 3.2 Description

### 3.2.1 Block Diagram

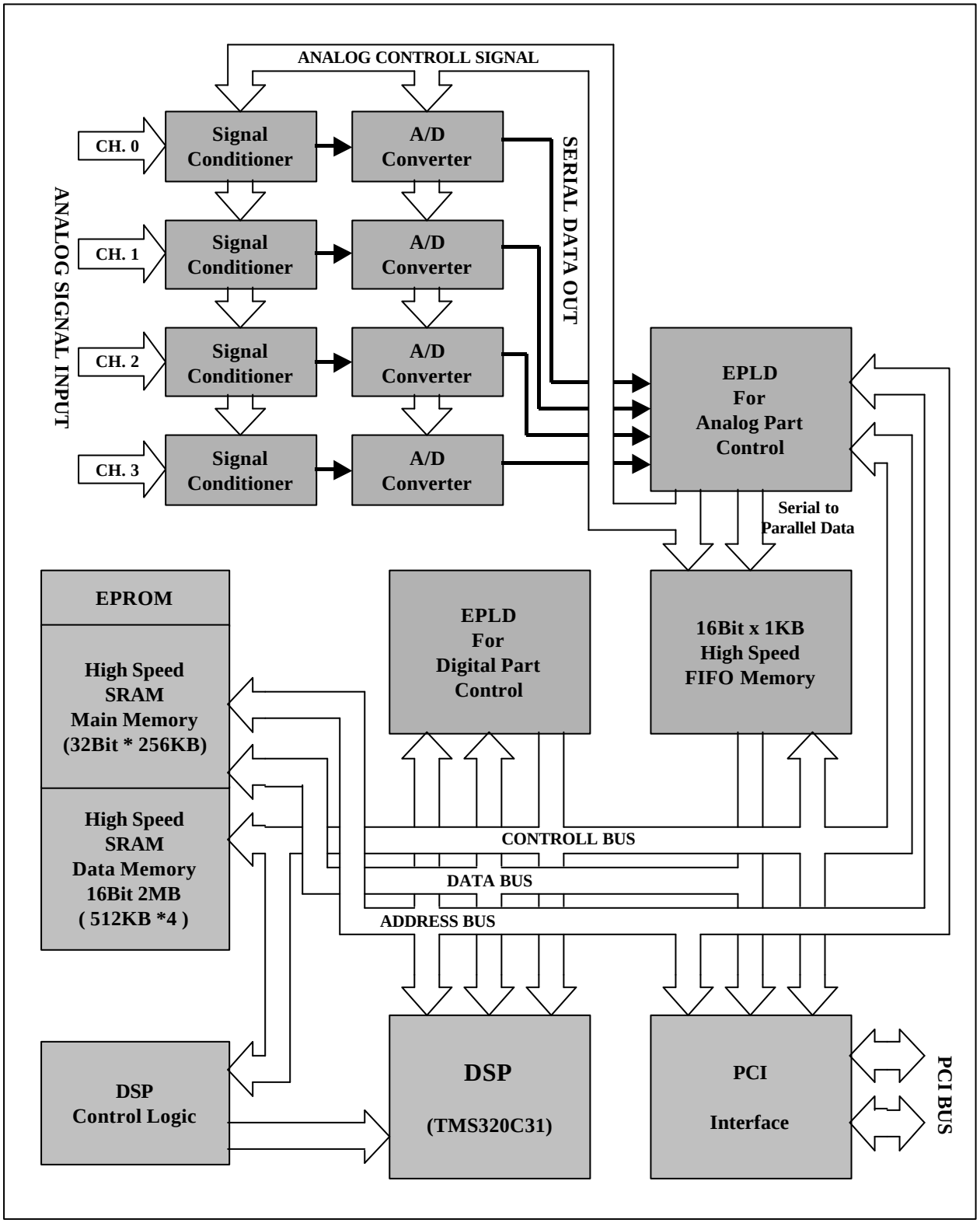



Figure 3-2 Board Block Diagram

### 3.2.2 General Description

Show brief description about block diagram to below.

1) DSP

TMS320C31 is used as DSP, and the function is

• performance

- 50 nsec singleness cycle instruction practice time
- 40 MFLOPS( Million Floating-point Operations Per Second )
- 20 MIPS( Million Instructions Per Second )

• 4K * 32 bit singleness cycle the inside ROM a territory

• two 1K * 32 bit cycle the inside RAW a territory

• 32 bit instruction/data word, 24bit address

• Internal DMA controller to execute I/O and CPU operation

• A motivated instructions for providing multiprocessing ( Interlocked )

2) PCI Interface

V360EPC-50 chipset is used as PCI interface.

This chipset consists of PCI Interface and local Interface.

3) Main Memory

Two high speed SRAM (16Bit x 256KB) is used as main memory.

Average access time is 15ns. This space is used as program running space.

4) EPROM

27C256 (8Bit x 32KB) is used as EPROM. There is booting program.

5) PLD

PLD decodes address, generates control signal in each chipset. It converts serial data to parallel data, saves data to FIFO memory. and, generates Interrupt.

6) FIFO Memory

IDT7282 (16Bit x 1KB) is used as high speed FIFO memory.

Access time is 12ns. It is used not to lose A/D conversion data of 4-Channel.

7) Signal Conditioner

PGA207 Op_AMP is used as signal conditioner.

Programmable Gain is 1,2,5,10 times.

8) A/D Converter 0-3

AD977 is used as A/D converter. It converts analog signal from Op-AMP to digital signal. Sampling speed of the AD977A chipset is maximum 200KHz, Resolution is 16Bit. Data outputs to serial interface, Analog input range is fixed to +-10V.

### 3.2.3 Digital Part

• Digital Parts consists of DSP(TMS320C31), PCI(V360EPC) and sub digital circuits.

## 1) DSP(TMS320C31)

• DSP address map is showed to below.

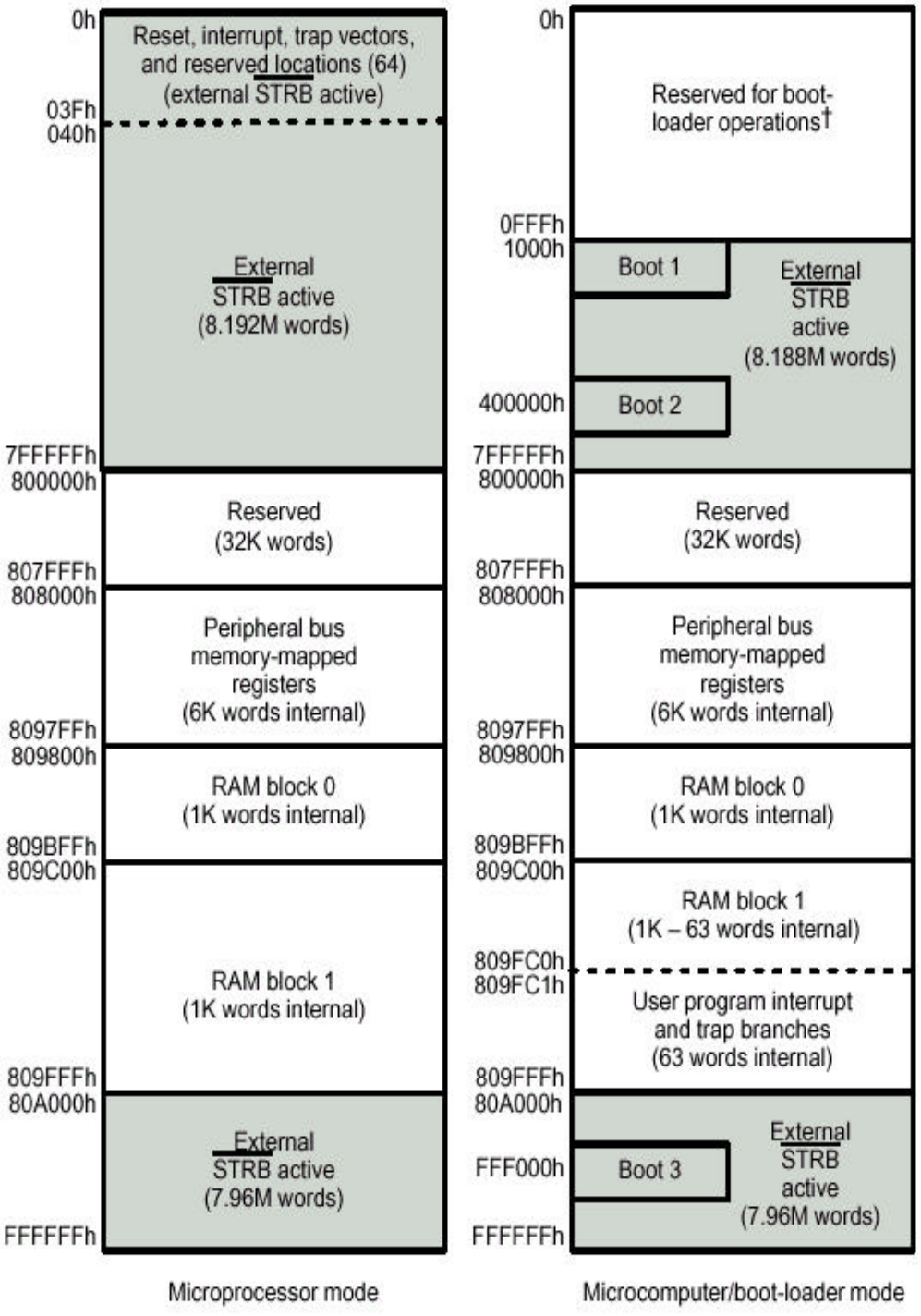



Figure 3-3 DSP Address Map

## 2) PCI Interface( V360EPC )

1) Memory address starts from 0EC01 0000h at PC side, and size is 256bytes.
(Start address is different at each PCI configuration cycle.)

2) V360EPC is booted by EEPROM(24C02).

- Device and Vender have to be equal to the Device and Vender of "dme_c3x.inf" file.
- Booting data of EEPROM is showed to below. (eeprom.d)

( if you want to update, it is possible to change in a new version.)

```
905010B5 00000003 905010B5 00000000
C0010000 FFFF0000 00000000 00000000
00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000100
80000002 00000000 00000000 00000000
00000000 00000000 00000000 00000000
00000000 00000000 00000000 02000000
00000000 00000000 0000C000 00000000
00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000
00000000 00000000 00000000 00000000
```

Figure 3-4 PCI Booting Data in EEPROM

- For details about all register of the V360EPC, refer to manual of V360EPC.
- For EEPROM write and read source (eeprom.c), contact to DongMyung Electronics.

3) PCI interface memory map is showed to next.

| REGISTER | | | | OFFSET |
|---|---|---|---|---|
| 31 | 16 | 15 | 0 | |
| PCI_DEVICE | | PCI_VENDOR | | 00H |
| PCI_STAT | | PCI_CMD | | 04H |
| PCI_CC_REV | | | | 08H |
| PCI_HDR_CFG | | | | 0CH |
| PCI_IO_BASE (PCI_I20_BASE when I20 operation is enabled: I20_EN bit) | | | | 10H |
| PCI_BASE0 | | | | 14H |
| PCI_BASE1 | | | | 18H |
| reserved | | | | 1C-2BH |
| PCI_SUB_ID | | PCI_SUB_VENDOR | | 2CH |
| PCI-ROM | | | | 30H |
| reserved | | | | 34-38H |
| PCI_BPARAM | | | | 3CH |
| PCI_MAP0 | | | | 40H |
| PCI_MAP1 (PCI_I20_MAP[a] when I20 operation is enabled: I20_EN bit) | | | | 44H |
| PCI_INT_STAT | | | | 48H |
| PCI_INT_CFG | | | | 4CH |
| reserved | | | | 50H |
| LB_BASE0 | | | | 54H |
| LB_BASE1 | | | | 58H |
| LB_MAP0 | | reserved | | 5CH |
| LB_MAP1 | | reserved | | 60H |
| LB_MAP2 | | LB_BASE2 | | 64H |
| LB_SIZE[b] | | | | 68H |
| LB_IO_BASE | | reserved | | 6CH |
| FIFO_PRIORITY | | FIFO_CFG | | 70H |
| LB_IMASK | LB_ISTAT | FIFO_STAT | | 74H |
| LB_CFG | | SYSTEM | | 78H |
| reserved | | PCI_CFG | | 7CH |
| DMA_PCI_ADDR0 | | | | 80H |
| DMA_LOCAL_ADDR0 | | | | 84H |
| DMA_CSR0 | DMA_LENGTH0 | | | 88H |
| DMA_CTLB_ADR0 | | | | 8CH |
| DMA_PCI_ADDR1 | | | | 90H |
| DMA_LOCAL_ADDR1 | | | | 94H |
| DMA_CSR1 | DMA_LENGTH1 | | | 98H |
| DMA_CTLB_ADR1 | | | | 9CH |
| I2O Message Unit Pointers[b] | | | | A0H - BCH |
| MAIL_DATA3 | MAIL_DATA2 | MAIL_DATA1 | MAIL_DATA0 | C0H |
| MAIL_DATA7 | MAIL_DATA6 | MAIL_DATA5 | MAIL_DATA4 | C4H |
| MAIL_DATA11 | MAIL_DATA10 | MAIL_DATA9 | MAIL_DATA8 | C8H |
| MAIL_DATA15 | MAIL_DATA14 | MAIL_DATA13 | MAIL_DATA12 | CCH |
| PCI_MAIL_IERD | | PCI_MAIL_IEWR | | D0H |
| LB_MAIL_IERD | | LB_MAIL_IEWR | | D4H |
| MAIL_RD_STAT | | MAIL_WR_STAT | | D8H |
| QBA_MAP | | | | DCH |
| | | | DMA_DELAY | E0H |

Figure 3-2 PCI Interface Memory Map

### 3.2.4 Memory Map

Table 3-3 Hardware Memory Map

| Memory Address | | Explain | Note |
|---|---|---|---|
| Begin | End | | |
| 0000:0000 | 000F:FFFF | Reserved | |
| 0010:0000 | 0010:2000 | Kernel, F/W, Stack | |
| 0010:2000 | 0010:5FFF | Ch0. Raw Data | 16K( integer ) |
| 0010:6000 | 0010:9FFF | Ch1. Raw Data | |
| 0010:A000 | 0010:DFFF | Ch2. Raw Data | |
| 0010:E000 | 0011:1FFF | Ch3. Raw Data | |
| 0011:2000 | 0011:5FFF | Ch0. FFT Data | 16K ( float ) |
| 0011:6000 | 0011:9FFF | Ch1. FFT Data | |
| 0011:A000 | 0011:DFFF | Ch2. FFT Data | |
| 0011:E000 | 0012:1FFF | Ch3. FFT Data | |
| 0012:2000 | 0012:5FFF | Sin Table | |
| 0012:6FFF | 0012:9FFF | Integer → floating | |
| | | | |
| 002F:F800 | 002F:FBFF | Interrupt vector table | |
| 002F:FC00 | 002F:FFFF | Kernel Program | |
| 0030:0000 | 003F:FFFF | Boot Loader EPROM | 256K x 8 |
| 0040:0000 | | EEPROM | 16KBit |
| 0050:0000 | | CTC | |
| 0070:0000 | | D/A | |
| 0080:0000 | | A/D | |
| 0084:0000 | | A/D MSB | |
| 0090:0000 | | MUX | |
| 0100:0000 | 3FFF:FFFF | Reserved | |
| 4000:0000 | 4000:FFFF | Local RAM | 64K x 32 |
| 8000:0000 | 800F:FFFF | Global RAM | 256K x 32 |
| 8010:0000 | 807F:FFFF | Reserved | |
| 007F:0000 | 007F:00FF | PCI Interface | 256Byte |
| 8080:0100 | FFFF:FFFF | Reserved | |

### 3.2.5 Analog Part

1. Analog part consists of signal conditioner, A/D converter and sub circuits.
2. A/D converter Block-diagram is showed to below.

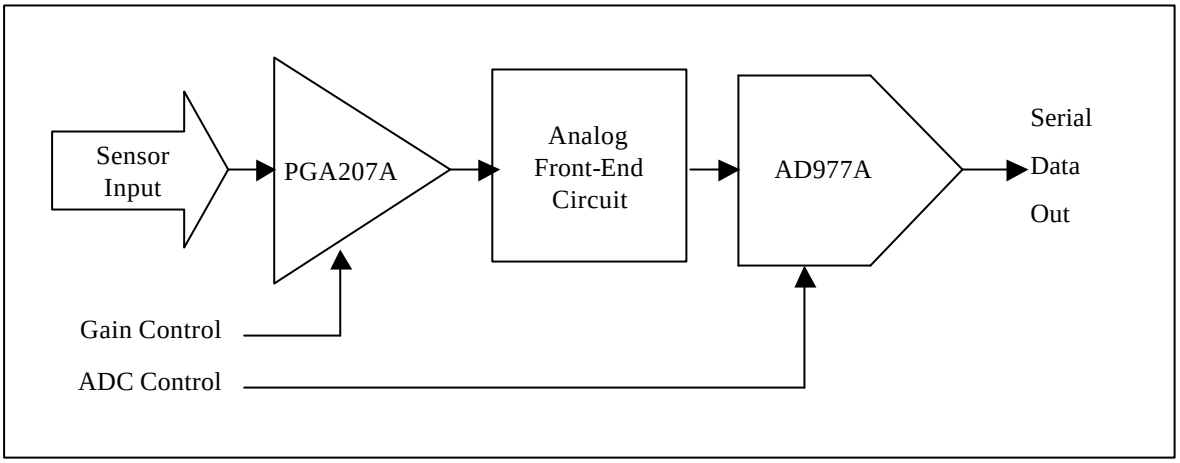



Figure 3-5 Analog Part Block Diagram

3. Explanation for circuits is shown to below.

1) Output signal from sensor connects to OP-Amp(PGA207A) input.
PGA207A OP-AMP input impedance is very high ($10^{13}$Ohm 1pF), it has +-40V input protection circuit, and it has programmable gain control (G=1,2,5,10), frequency response characteristic is about 600KHz ~ 5MHz. And minimum slew rate is about 25V/uS, so, it is suitable for buffer.

2) Output signal from AMP connects to Analog Front-End circuit for adjust +-10V input range.

3) Output signal from Analog Front-End Circuit connects to AD977A for analog to digital conversion.

4) AD977A has a 16Bit, 200kBPS analog to digital conversion capacity.
It supports high speed serial interface.
Serial output data from ADC connects to high speed PLD for two bytes data conversion.
Conversion data is stored FIFO memory. and DSP processes high speed digital signal processing.

## 3.3 Board VHDL

The part of VHDL Source code is showed to below.

Contact to Dongmyung Electronics for the question of VHDL source code.

```
--                                  3th edition
--                                  c31.vhd for C31 4-Channel A/D Board
--                                  DongMyung Electronics Co., ltd.   2001/03/02

library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity c31c is
port(
                    la              :in  std_logic_vector(23 downto 0);
                    ld              :inout std_logic_vector(15 downto 0);
…….
…….
begin
                    xa    <= la(7) &la(6) &la(5) &la(4) &la(3) &la(2) &la(1) &la(0);
                    addrh <= la(23) &la(22) &la(21) &la(20) &la(19) &la(18) &la(17) &la(16);
                    xis <= '0' when ( holda='1' and addrh="00110000" ) else '1';
…….
…….
                    dcnt := dcnt + 1;
                    else
                                        ld <= "ZZZZZZZZZZZZZZZZ";
                                        dcnt := 0;
                                        end if;
                    end if;
                    end process gen_fifo_wr;
end main;
```

Figure 3-6 VHDL Source Code Example

## 3.4 Firmware

### 1) Booting Part( File Down Loader )

- Booting device is EPROM(27C256).
- The contents of ROM is File Down loader.
- Contact to DongMyung Electronics for the source code of ROM.

### 2) Command Part( Sender, Receive )

- Mail Box0 is used to send command from Host to DSP.
- Mail Box2 is used to send command from DSP to Host.
- Command Spec(32Bit) is showed to below.

Table 3-4 Command Spec

| No. | Command | Hex Code | Function |
|---|---|---|---|
| 1 | Auto Mode ( include A/D Start ) | 0x10 | Host -> Target data transfer |
| 2 | Trigger Mode ( " ) | 0x11 | Host -> Target data transfer |
| 3 | A/D Begin | 0x12 | Host -> Target data transfer |
| 4 | A/D Stop | 0x13 | Host -> Target data transfer |
| 5 | Check Point | 0x30 | |
| 6 | GAIN CH | 0x40 | • 0 CH : 0x10 ~ 0x13<br>• 1 CH : 0x20 ~ 0x23<br>• 2 CH : 0x40 ~ 0x43<br>• 3 CH : 0x80 ~ 0x83<br># Gain<br>. X0 : 1<br>. X1 : 2<br>. X2 : 5<br>. X3 : 10 |
| 7 | Frequency Install | 0x50 | Timer Install |
| 8 | Frequency Reset | 0x51 | Timer Reset |
| 9 | Frequency Setup | 0x52 | Timer Setup |
| 10 | Down OK | 0xEE | Target -> Host data transfer |
| | | | |

### 3) Data Tx, Rx Part( Sender, Receiver )

- Send and receive large data from Host to DSP.
- Data specification is 32bit.
- For use, open the apertures.

### 4) H/W Dignostic and Driver Part

- Memory : read, write test
- Timer : on, off timer or count.
- Amplifier : amplifier input signal.
- A/D : convert analog signal to digital signal.

## 3.5 VxD Description

The part of VxD Source code is showed to below.

Contact to Dongmyung Electronics for the question of VxD source code.

```
//////////////////////////////////////////////////////////////////////////
//   VDASD.C -- Main code for C3x DSP Data Acquisition Device Driver
//   Use with C9 (32-bit) and MASM 6.11c from DDK
//   Copyright 2000 DongMyung Electronics Co., Ltd.
//////////////////////////////////////////////////////////////////////////

#define WANTVXDWRAPS  // C language coding
#include <basedef.h>
#include <vmm.h>
#include <debug.h>
……
……
                CM_Add_Empty_Log_Conf(&logconf, device, LCPRI_NORMAL,BASIC_LOG_CONF
| PRIORITY_EQUAL_LAST);
                CM_Add_Res_Des(&resource, logconf, ResType_IRQ,          &irq1,
sizeof(irq1), 0);
……
……
                case CARD_INFO:
                        CM_CallBack_Enumerator(OnEnumerate, 0);
                        plai1 = (PLAI)p ->lpvInBuffer;
                        LAI.ladi_dwMemBase[3] = plai1->ladi_dwMemBase[3];
                        plai1 = (PLAI)p ->lpvOutBuffer;
                        plai1->ladi_bIRQ = LAI.ladi_bIRQ;
                        plai1->ladi_dwIRQHandle = LAI.ladi_dwIRQHandle;
```

Figure 3-7 VxD Source Code Example

# Appendix

This chapter include

A. Specification

B. Component List

C. Device Data Sheets

# A. Specification

Table A-1 Board Specification

| Item | Spec. | Note |
|---|---|---|
| Processor | 1. CPU : DSP-TMS320C31<br>2. Speed : 40 MHz<br>3. Serial Port : 1 Port<br>4. Timer : Timer 1 | |
| Processor Memory | 1. Program Memory : 256K * 32 Bits<br>2. Data Memory : 2M * 16 Bits | |
| Amplifier | 1. PGA207<br>. DIGITALLY PROGRAMMABLE GAINS:<br>. PGA207: G=1, 2, 5, 10V/V<br>. TRUE INSTRUMENTATION AMP INPUT<br>. FAST SETTLING: 3.5ms to 0.01%<br>. FET INPUT: I B = 100pA max<br>. INPUT PROTECTION: +-40V<br>. LOW OFFSET VOLTAGE: 1.5mV max<br>. 16-PIN DIP, SOL-16 SOIC PACKAGES | |
| FIFO Memory | 1. Size : 1K * 16 Bits<br>. The 7285 is equivalent to two 7205 8,192 x 9 FIFOs<br>. Low power consumption<br>*- Active: 685 mW (max.)*<br>*-. Power-down: 83 mW (max.)*<br>. Ultra high speed —12 ns access time<br>. Asynchronous and simultaneous read and write<br>. Offers optimal combination of data capacity, small foot print and functional flexibility<br>. Ideal for bi-directional, width expansion, depth expansion, bus-matching, and data sorting applications<br>. Status Flags: Empty, Half-Full, Full<br>. Auto-retransmit capability<br>. High-performance CMOS technology<br>. Space-saving TSSOP<br>. Industrial temperature range (–40 o C to +85 o C) is available | |

# A. Specification (Continued)

| Item | Spec. | Note |
|---|---|---|
| Command Port | 1. 32Bits | |
| Input Amplifier | 1. Chip : PGA207A<br>2. Input Voltage Protection : -40V ~ +40V<br>3. Input Impedance : $10^{13}$Ohm 1pF<br>4. Temperature Coefficient : 25PPM/C(Max.) | |
| Analog to Digital | 1. Chip :AD977AARS<br>2. Resolution : 16 Bit (Include Sing Bit )<br>3. Input Range : -10V ~ +10V<br>4. Maximum Reading Rate : 200KSample/sec | |
| Power source | +-5, +-15 Volt | |
| PCB | 305x114mm 6 layer epoxy resins board | |

# B. Component List

## B.1 Processor Part

Table B-1 Processor Part Component List

| No | Part | Quantity | Note |
|---|---|---|---|
| 1 | 1K Array Resistor | 1 | |
| 2 | 0.1uF | 59 | SMD type |
| 3 | 0.1uF | 2 | " |
| 4 | POWER LED | 1 | " |
| 5 | RESET LED | 1 | " |
| 6 | HEADER 30 * 2 | 1 | Connector |
| 7 | HEADER 5 * 2 | 1 | " |
| 8 | HEADER 3 * 2 | 1 | " |
| 9 | HEADER 4 | 1 | " |
| 10 | 4.7k | 20 | |
| 11 | 10k | 4 | |
| 12 | 120ohm | 1 | |
| 13 | 180ohm | 1 | |
| 14 | 330ohm | 2 | |
| 15 | 2.2K | 1 | |
| 16 | INOR | 1 | |
| 17 | 74F74 | 4 | |
| 18 | 74F245 | 1 | |
| 19 | TMS320C31/PFP | 1 | DSP, Maker TI |
| 20 | 40MHz | 1 | Oscillator |
| 21 | 74F08 | 1 | Logic device |
| 22 | 74F04 | 1 | " |
| 23 | 74F175 | 1 | " |
| 24 | EMP7256SRC208-15 | 1 | EPLD, Maker ALTRA |
| 25 | 27C256 | 1 | EPROM |
| 26 | KM616V4002B-15 | 2 | SRAM |
| 27 | V360EPC_P | 1 | PCI Controller, Maker V3 |
| 28 | AT24C02N | 1 | EEPROM |
| | | | |

## B.2 Analog Part

Table B-2 Analog Part Component List

| No | Part | Quantity | Note |
|---|---|---|---|
| 1 | 1K | 5 | |
| 2 | 0.1 uF | 39 | |
| 3 | 10 uF | 6 | |
| 4 | 2.2uF | 8 | |
| 5 | 47uF, 25V | 2 | |
| 6 | HEADER 30*2 | 1 | Connector |
| 7 | BNC | 4 | “ |
| 8 | PLD HEADER | 1 | “ |
| 9 | 50ohm | 16 | |
| 10 | 200ohm | 4 | |
| 11 | 100ohm | 8 | |
| 12 | 33K,576K | 4 | |
| 13 | 4.7K | 1 | |
| 14 | 10K | 4 | |
| 15 | PGA207 | 4 | AMP |
| 16 | AD977AARS | 4 | ADC, Maker AD |
| 17 | EPM7256SRC208-15 | 1 | EPLD, Maker ALTRA |
| 18 | 74F14 | 1 | Logic device |
| 19 | IDT7282L/SO | 1 | Fifo memory |
| 20 | IWD515 | 1 | |
| 21 | LM7805C/TO220 | 1 | |
| 22 | LM7905C/TO220 | 1 | |
| 23 | 100 pF, 50 K | 8 | |
| 24 | 200 K | 4 | |

# C. Device Data Sheets

The Follow devices provides data sheets.

1. V360EPC
2. AD977A
3. PGA207
4. EMP7256SRC208
5. IDT7282L